VERSION SHOWING THE CHANGES TO THE SPECIFICATION

(TRANSLATION)

IN THE SPECIFICATION

Amend the specification as follows:

Page 1, line 1, ~~Description~~

Page 5, lines 27-37:

Ffigure 1 shows two layouts for an OFET;

Ffigures 2, 2A and 2B show[[s]] two layouts for an inverter;

Ffigure 3 shows one layout for a two-input NOR gate;

Ffigure 4 shows one layout for a two-input NAND gate; and

Ffigure 5 shows one layout for a five-stage ring oscillator.

Page 6, lines 9-12:

Figure 1 ~~1a~~ shows the simplest embodiment, in which a U-shaped current channel (OFET channel 3) is formed, and figure 1b) shows a somewhat more elaborate embodiment, in which a meandering OFET channel 3 is formed.

Page 6, line 24 to page 7, line 10:

Figure 2A ~~2a)~~ shows an inverter having a load OFET at the output: the inverter comprises two OFETs, the load OFET and the drive OFET. The source electrode 1 of the load OFET surrounds the drain electrode 2 of the load OFET on three sides and an OFET channel 3, which is covered by the gate electrode 13 of the load OFET, is produced,

another part of the source electrode 1 and of the drain electrode 2 of the load OFET also being concomitantly covered. In addition, the gate electrode 13 is connected not only to the source electrode 2 but also to the output 11 and to the source electrode 7 of the drive OFET via the through-contact 10. The gate electrode 8 of the drive OFET covers the channel 6 of the drive OFET and is connected to the input 12. The drain electrode 5 of the drive OFET surrounds the source electrode 7 and thus defines the channel 6. The holes or interruptions 9 in the semiconductor layer are situated between the load and drive OFETs and prevent leakage currents. The supply voltage is applied to electrode 1 and electrode 5 is at ground. These two electrodes surround virtually the entire inverter and thereby shield it from other components. When changing over the inverter, only the potential of electrode 2 or 7 changes, said electrodes being connected to one another and being situated in the interior of the inverter.

Page 7, lines 18-27:

The example of an inverter shown in figure 2B ~~2b)~~ has the load OFET gate at the supply voltage. The design is analogous to that from figure 2A ~~2a)~~. In contrast ~~to~~to the inverter of Fig. 2A ~~2a)~~, the gate electrode 13 is connected, in this case, to the source electrode 1 by means of the through-contact 10a and not, as in Fig. 2A ~~2a)~~, to the through-contact 10a to the output 11. The through-contact 10b is elongated as far as the edge of electrode 1, thus having the advantage that inverters which are located next to one another can jointly use the through-contact.

Page 7, line 36 to page 8, line 35:

Figure 3 shows one layout for a two-input NOR gate: the layout essentially corresponds to that of the inverter from figure 2B ~~2b)~~ with the difference that two drive OFETs are connected in parallel. The second drive OFET comprises the source electrode 14 and has a joint drain electrode 5 with the first drive OFET. The gate electrode 15 of the drive OFET is connected to the second input 12b of the NOR gate. The entire NOR gate is shielded by the two electrodes 1 and 5 which are at the supply voltage or ground.

Figure 4 shows a two-input NAND gate. The NAND layout likewise essentially corresponds to the inverter from figure 2B ~~2b)~~ with the difference that two drive OFETs are connected in series. The second drive OFET is surrounded by the first on three sides. The source electrode 7 of the first drive OFET is simultaneously the drain electrode of the second drive OFET. The source electrode 14 determines the channel 16 of the second drive OFET and is covered by the gate electrode 15, which is connected to the second input 12a. In this layout too, there is shielding by the electrodes 1 and 5.

Finally, figure 5 shows a five-stage ring oscillator comprising five inverters which are designed as shown in figure 2B ~~2b~~. The inverters are arranged in such a manner that, in the center, a joint through-contact 10 (10b) can be used for all of the inverters. In addition, the inverters are arranged in such a manner that they butt against one another directly, this

only being possible as a result of the layout according to the invention. The inverters are connected at the ends by means of the connecting lines 17 and the holes or interruptions in the semiconductor 9 are also continued between the connecting lines in order to prevent leakage currents. The output 11 of the ring oscillator branches off at a connecting line 17.